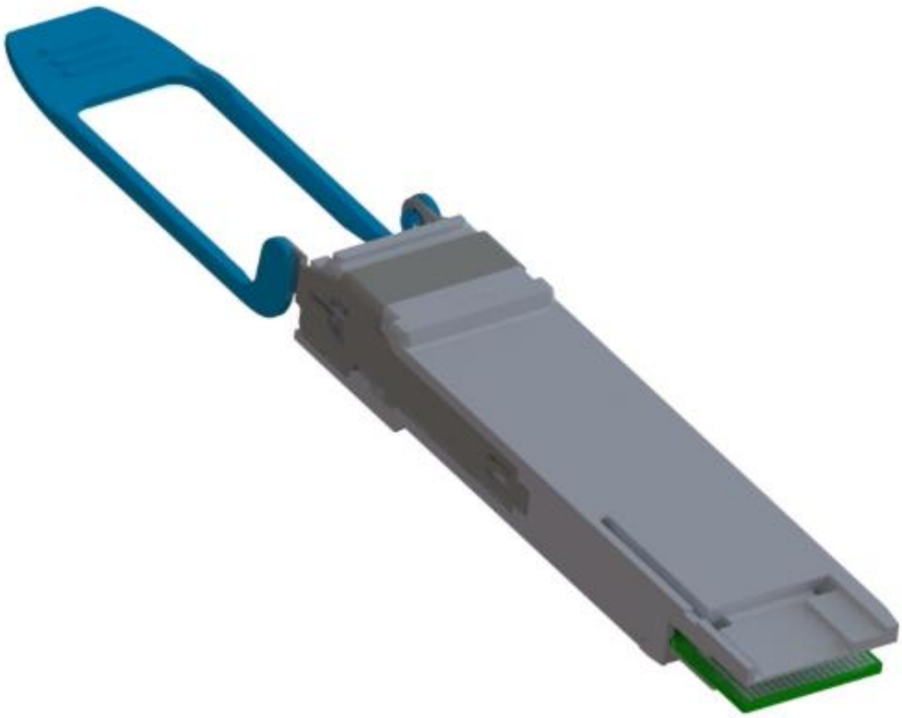
ML3062-SLB-56-14W-V6

Technical Reference

QSFP-DD Electrical Passive Loopback Module

CMIS 4.0 Compliant



Innovation for the next generation

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Innovation for the next generation

1 Overview

The **ML3062-SLB-56-14W-V6** is used for testing QSFP-DD transceiver ports under board level tests, by substituting main QSFP-DD transceiver features.
The **ML3062-SLB-56-14W-V6** is packaged in a standard MSA housing compatible with all QSFP-DD ports.
Note that the **ML3062-SLB-56-14W-V6** follows the **CMIS Rev 4.0** standard.

1.1 ML3062-SLB-56-14W-V6 QSFP-DD Passive Loopback Module | Key Features

- Supports 8x56G electrical interface
- QSFP-DD MSA Form Factor
- Built with advanced PCB material
- Power consumption set to 14.44 W
- Temperature Monitor
- Superior SI performance
- MSA Compatible Configuration and EEPROM
- Loops back TX to RX on all 8 ports
- I2C Interface
- 2 status LED Indicator
- Hot Pluggable module
- Cut-off temperature preventing module overheating

1.2 LED Indicator

Green (Solid) – Signifies that the module is operating in high power mode.
Red (Solid) – Signifies the module is operating in low power mode.
Green (Blinking) – Module in high power mode and Temperature Alarm is triggered.

1.3 Recommended Operating Conditions

Parameter	Symbol	Notes/Conditions	Min	Typ	Max	Units
Operating Temperature	T_A		-40		85	°C
Supply Voltage	VCC	Main Supply Voltage	3.00	3.3	3.6	V
Input/output Load Resistance	RL	AC-Coupled, Differential	90	100	110	Ω
Power Class		Programmable to Emulate all power classes	0	14.44		W

Bit Rate		28G NRZ 56G PAM4			56	Gbps

2 Functional Description

2.1 Management Data Interface – I2C

The **ML3062-SLB-56-14W-V6** supports the I2C interface.

2.2 I2C Signals, Addressing and Frame Structure

2.2.1 I2C Frame

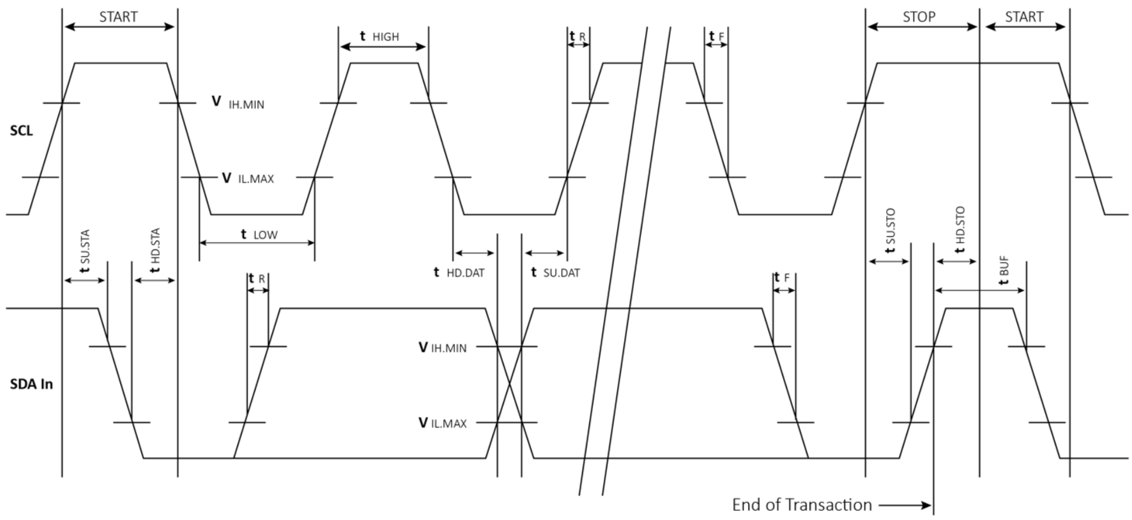

Figure 1: QSFP-DD Timing Diagram

Before initiating a 2-wire serial bus communication, the host will provide setup time on the ModSelL line of all modules on the 2-wire bus. The host will not change the ModSelL line of any module until the 2-wire serial bus communication is complete and the hold time requirement is satisfied. The 2-wire serial interface address of the QSFP-DD module is 1010000X (A0h).

In order to allow access to multiple QSFP-DD modules on the same 2-wire serial bus, the QSFP-DD pin-out includes a module select pin (ModSelL). This pin (which is pulled high in the module) must be held low by the host to select the module of interest and allow communication over the 2-wire serial interface. The module do not respond to or accept 2-wire serial bus instructions unless it is selected.

2.2.2 Management Timing Parameters

The timing parameters for the 2-Wire interface to the QSFP-DD module are shown in the table below:

Parameter	Symbol	Min	Max	Unit
Clock Frequency	f_{SCL}	0	400	kHz
Clock Pulse Width Low	t_{LOW}	1.3		us
Clock Pulse Width High	t_{High}	0.6		us
Time bus free before new transmission can start	t_{BUF}	20		us
START Hold Time	$t_{HD.STA}$	0.6		us
START Set-up Time	$t_{SU.STA}$	0.6		us
Data In Hold Time	$t_{HD.DAT}$	0		us
Data in Setup Time	$t_{SU.DAT}$	0.1		us
Input Rise Time (400 kHz)	$t_{R.400}$		300	ns
Input Fall Time (400 kHz)	$t_{F.400}$		300	ns
STOP Set-up Time	$t_{SU.STO}$	0.6		us
ModSelL Setup Time	$t_{SU.ModSelL}$	2		ms
ModSelL Hold Time	$t_{HD.ModSelL}$	2		ms
Aborted sequence – bus release	Deselect_Abort	2		ms

2.2.3 Memory Specifications

QSFP-DD memory transaction timings are given in the following table.

Parameter	Symbol	Min	Typ	Max	Unit
Serial Interface Clock Holdoff "Clock Stretching"	T_clock_hold			500	us
Complete Single Write	tWR			5	ms
Endurance (Write Cycles)		50K			cycles

2.2.4 Device Addressing and Operation

Clock and Data Transitions: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods indicate a START or STOP condition. All addresses and data words are serially transmitted to and from the QSFP-DD in 8-bit words.

Every Byte on the SDA line must be 8-bits long. Data is transferred with the most significant bit (MSB) first.

START Condition: A high-to-low transition of SDA with SCL high is a START condition, which must precede any other command.

STOP Condition: A low-to-high transition of SDA with SCL high is a STOP condition.

Acknowledge: After sending each 8-bit word, the transmitter releases the SDA line for one-bit time, during which the receiver is allowed to pull SDA low (zero) to acknowledge (ACK) that it has received each word.

Memory (Management Interface) Reset: After an interruption in protocol, power loss or system reset the QSFP-DD Module management interface can be reset. Memory reset is intended only to reset the QSFP-DD transceiver management interface (to correct a hung bus). No other module functionality is implied.

Clock up to 9 cycles

Look for SDA high in each cycle while SCL is high

Create a Start condition as SDA is high

Device Addressing: QSFP-DD devices require an 8-bit device address word following a start condition to enable a read or write operation. The device address word consists of a mandatory sequence for the first seven most significant bits in Figure 2. This is common to all QSFP-DD devices.

1	0	1	0	0	0	0	R/W
MSB							LSB

Figure 2: QSFP-DD Device Address

The eighth bit of the device address is the read/write operating select bit. A read operation is initiated if this bit is set high and a write operation is initiated if this bit is set low. Upon compare of the device address (with ModSelL in the low state) the QSFP-DD Module will output a zero (ACK) on the SDA line to acknowledge the address.

2.3 QSFP-DD Memory Map

2.3.1 Full Map

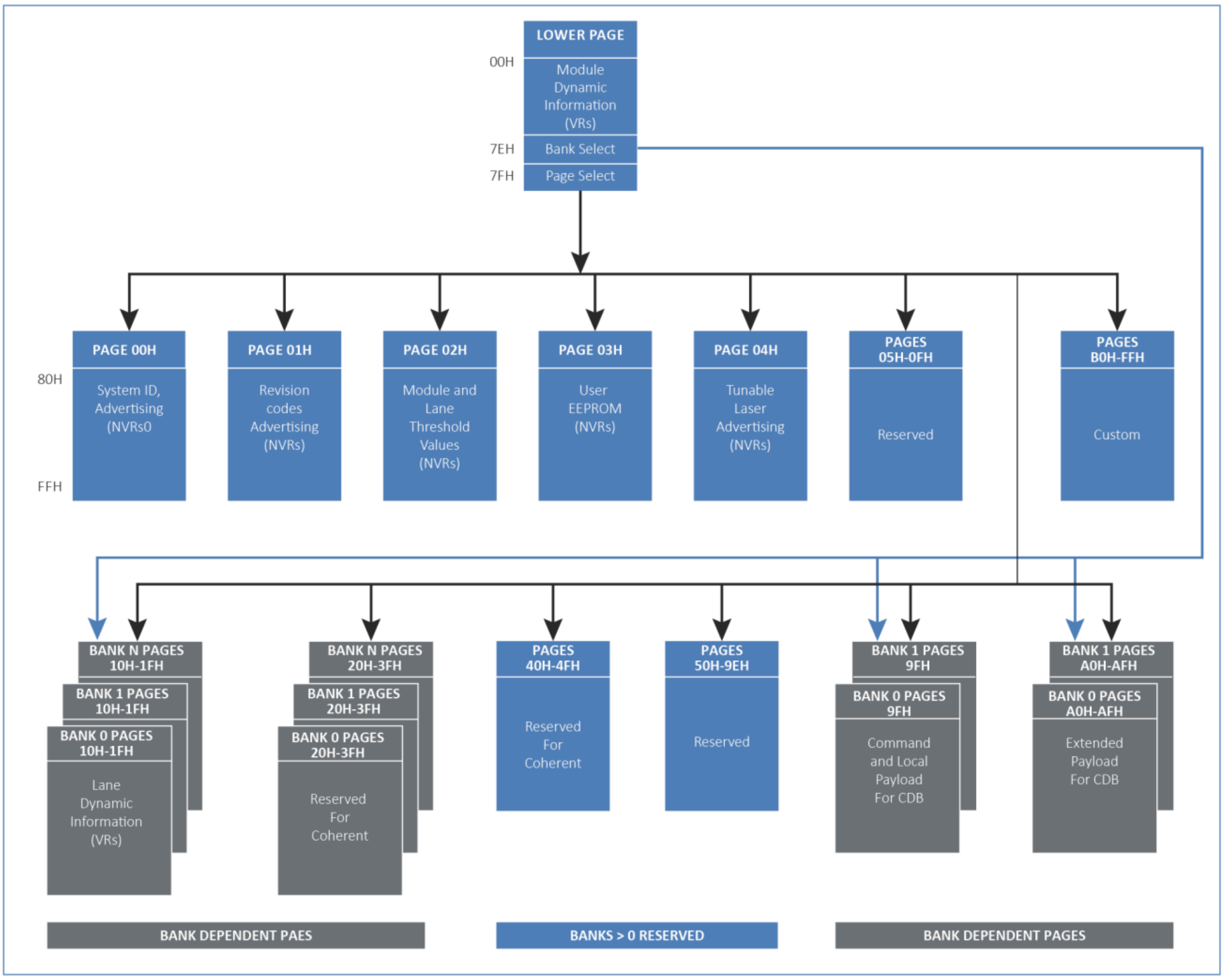

Figure 3: QSFP-DD Memory Map

This section defines the Memory Map for QSFP-DD transceiver used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all QSFP-DD devices.
The structure of the memory is shown in Figure 3. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, e.g. Interrupt Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings are available with the Page Select function. The structure also provides address expansion by adding additional upper pages as needed.

2.3.2 ML3062- SLB-56-14W-V6 Memory Map

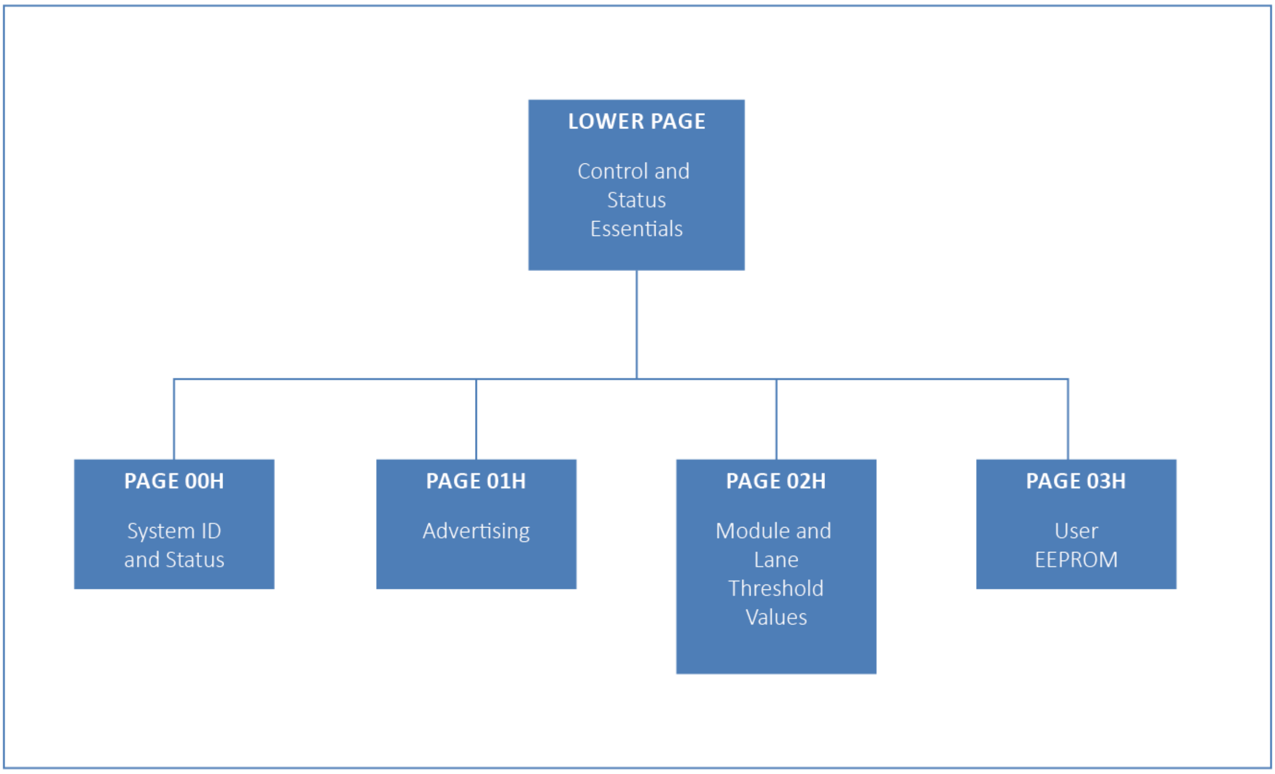

Figure 4: Implemented Memory Map

2.3.3 Memory Accessibility

The Memory Map registers types are shown in the table below:

Page Address	Address Range	Type
Lower Page	0-25	RO
	26	RW (VR)
	27-126	RO
	127	RW (VR)
Page 00h	128-165	RO
	166-181	RW (NVR)
	182-255	RO
Page 01h	128-255	RO
Page 02h	128-255	RO
Page 03 Lower Page	128-131	RW (NVR)
	132-133	RO
	134-138	RW (NVR)
	139	RW
	140-151	RW (NVR)
	152-159	RO

	160-255	RW (NVR)
	0-25	RO
	26	RW (VR)

2.4 Low Speed Electrical Hardware Pins

In addition to the 2-wire serial interface the module has the following low speed pins for control and status:

- ModselL
- ResetL
- LPMode
- IntL
- ModPrsL

2.4.1 ModselL

The ModSelL is an input signal to the module that is pulled up to Vcc in the QSFP-DD module. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP-DD modules on a single 2-wire interface bus. When ModSelL is "High", the module will not respond to or acknowledge any 2-wire interface communication from the host.

2.4.2 ResetL

ResetL, is an active-low signal, and must be asserted for longer than the minimum reset pulse duration to trigger a module reset.

2.4.3 LPMode

LPMode is an input signal to the module from the host, operating with active high logic. The LPMode signal is pulled up to Vcc in the QSFP-DD module through a 4.75 kOhm resistor. The LPMode signal intervenes in the Module State Transition (refer to section 2.5.1 for more details).

2.4.4 IntL

IntL is an output signal. When the IntL signal is asserted Low it indicates a change in module state, a possible module operational fault or a status critical to the host system. The IntL signal is deasserted "High" after all set interrupt flags are read.

2.4.5 ModPrsL

ModPrsL is grounded in the module. The ModPrsL is asserted "Low" when the module is inserted and deasserted "High" when the module is physically absent from the host connector.

2.5 ML3062-SLB-56-14W-V6 Specific Functions

2.5.1 Module State Transition

The state transition between Low-Power and High-Power is related to three parameters:

1. ForceLowPwr bit– software control (forces module into low power mode), register 26 bit 4
2. LowPwr bit – software control, register 26 bit 6
3. LPMode – Hardware signal

According to these parameters, the state of the module is defined. Conditions for Low Power and High Power state, are summarized in the table below.

ForceLowPwr (Reg 26 bit 4)	LowPwr (register 26 bit 6)	LPMode	State
1	X	X	Low Power
0	1	1	Low Power
0	1	0	High Power
0	0	1	High Power
0	0	0	High Power

2.5.2 Module Global Controls

Module global controls are control aspects that are applicable to the entire module on all channels in the module.

Address	Bit	Name	Description	Type
26 (lower Page)	6	LowPwr	Parameter used to control the module power mode (refer to section 2.5.1) Default value =1	RW
	4	ForceLowPwr	0b = high power mode(default) 1b =Forces module into low power mode	
	3	Software Reset	Self-clearing bit that causes the module to be reset. The effect is the same as asserting the reset pin for the appropriate hold time, followed by its de-assertion. This bit will be cleared to zero on a reset so a value of 0 will always be returned. 0b = not in reset 1b = Software reset	
3 (lower page)	0	Software Interrupt	Digital state of Interrupt: 0b = Interrupt source is present 1b = No interrupt source present	RO

2.5.3 Temperature Monitor

The **ML3062-SLB-56-14W-V6** has 2 internal temperature sensors, on the PCBA, in order to continuously monitor the module’s temperature. Internally measured Module temperature are represented as a 16-bit signed two's complement value in increments of 1/256 degrees Celsius, yielding a total range of –127° C to +128° C that is considered valid between –40 and +125° C.

Address	Bit	Name	Description	Type
14 (lower Page)	All	Temperature MSB	Internally measured module temperature 3	RO
15 (lower Page)	All	Temperature LSB	Internally measured module temperature 3	
24 (lower Page)	All	Custom Temperature MSB	Internally measured module temperature 1	
25 (lower Page)	All	Custom Temperature LSB	Internally measured module temperature 1	

The distribution of internal temperature sensors is shown in the figure 5.

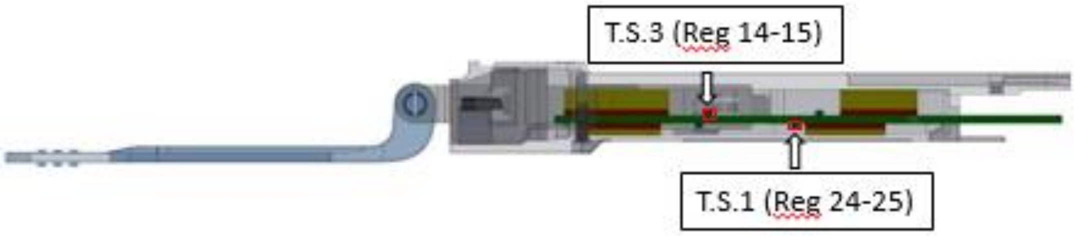

Figure 5: Temperature sensor location

The temperature High Alarms interrupt flag exists in lower page.

Address	Bit	Name	Description	Type
9 (lower Page)	0	L-Temp High Alarm	Latched high temperature alarm flag	RO

Note that any interrupt flag when asserted will generate the interrupt. Its state is read from register 3 bit 0.

2.5.4 Power Dissipation

The module contains 4 thermal spots positioned where the optical transceivers usually are in an optical module. The distribution of these spots is shown in the image below (Figure 6).

The consumed power is set to 14.44 W by default (only in high power mode). In Low power mode the module automatically turns off all power spots.

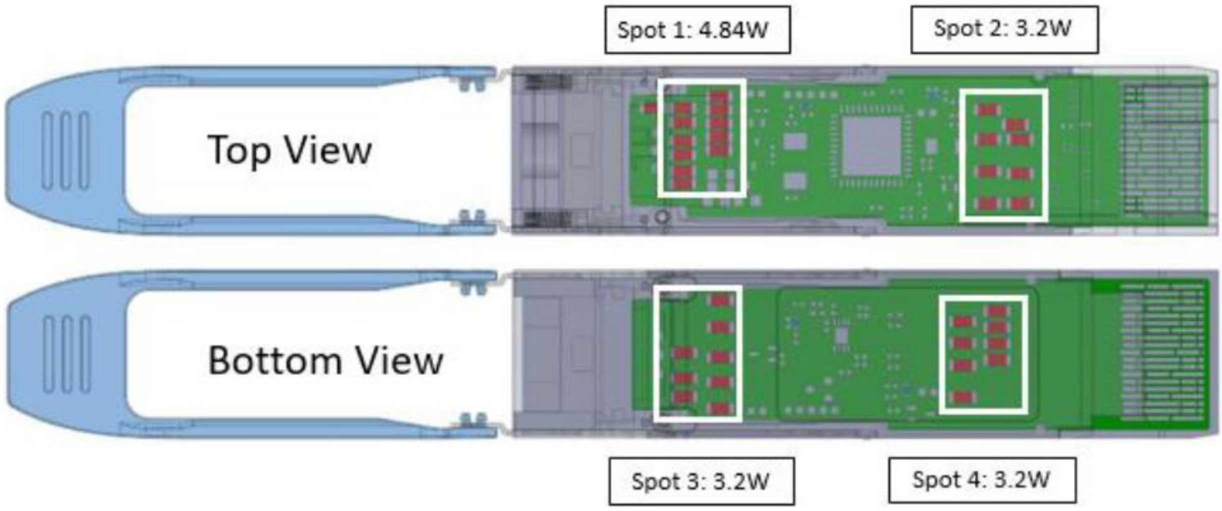

Figure 6: Thermal spots distribution

Figure 7 shows a side view of the distribution of thermal spots and TIM. Red shapes are the heat spots at the top and bottom of the PCB, and the yellow shapes are TIM for heat conduction to the shell. The TIM conductivity is 3 W/m.K.

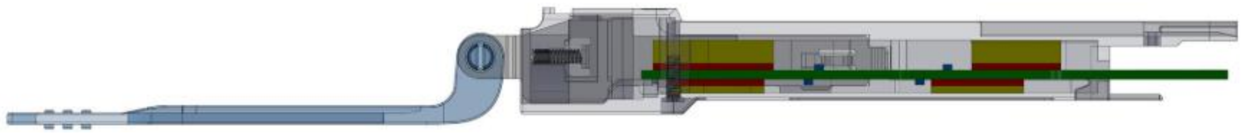

Figure 7: Module side view

2.5.5 Cut-Off Temperature

To avoid overheating the module, a Cut-Off Temperature is pre-defined.
The module is continuously monitoring the temperature and checking its value against the Cut-Off temperature. Once the module temperature reaches the cut-off temperature, all power spots will automatically turn off in order to prevent overheating. Once the temperature is 5 degrees below cut-off value, previous values are reloaded to all control registers.
The Cut-Off temperature for the **ML3062-SLB-56-14W-V6** is set to 85˚C.

2.5.6 Alarm Threshold

The temperature has a high alarm threshold. This factory preset value allows the user to determine when the temperature exceeds the predefined limit. The temperature LSB unit is 1/256 ˚C. Note that these addresses are of memory Page 02.

Address	Bit	Name	Default Value	Type
128(Page 02)	ALL	high temp alarm threshold (MSB)	80˚C	RO
129(Page 02)	ALL	high temp alarm threshold (LSB)		

2.5.7 FW and HW Revision

Information about the FW and HW revision are present in Lower Page, registers 39-40, and in Page01 registers 130-131, respectively, as described in the table below.

Address	Bit	Description	Type
39 (Lower Page)	All	Major FW Rev	RO
40 (Lower Page)	All	Minor FW Rev	
130 (page 01)	All	Major HW Rev	
131 (page 01)	All	Minor HW Rev	

3 High Speed Signals

High speed signals are electrically looped back from TX side to RX side of the module, all differential TX pairs are connected to the corresponding RX pairs, and the signals are AC coupled as specified by QSFP-DD MSA High Speed Electrical specs.
The Passive traces connecting TX to RX pairs are designed to support a data rate up to 56 Gbps.

4 QSFP-DD Pin Allocation

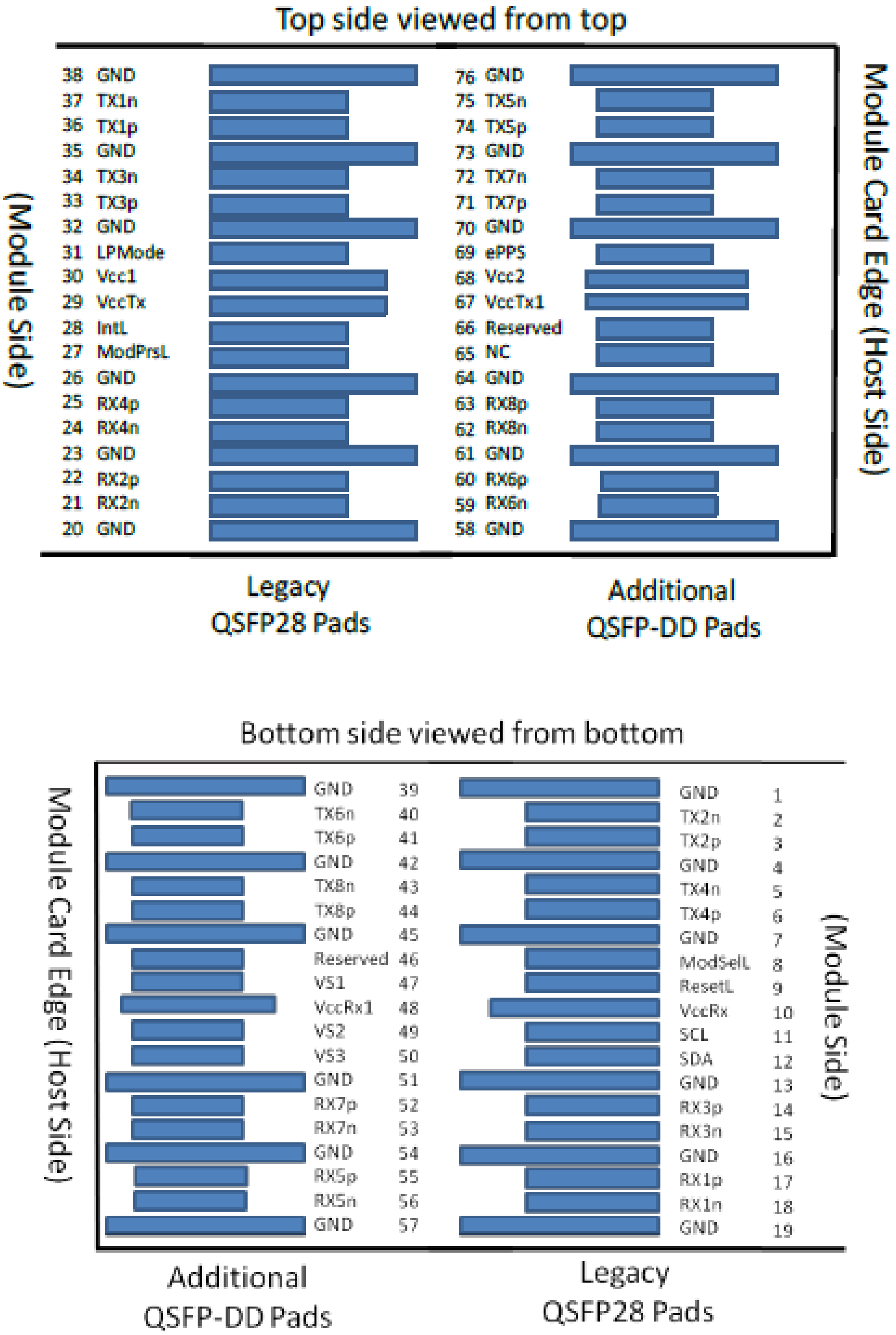

Figure 8: QSFP-DD Module Pad Layout

5 Mechanical Dimensions

A general description of mechanical dimensions of the **ML3062-SLB-56-14W-V6** is shown in the image below.

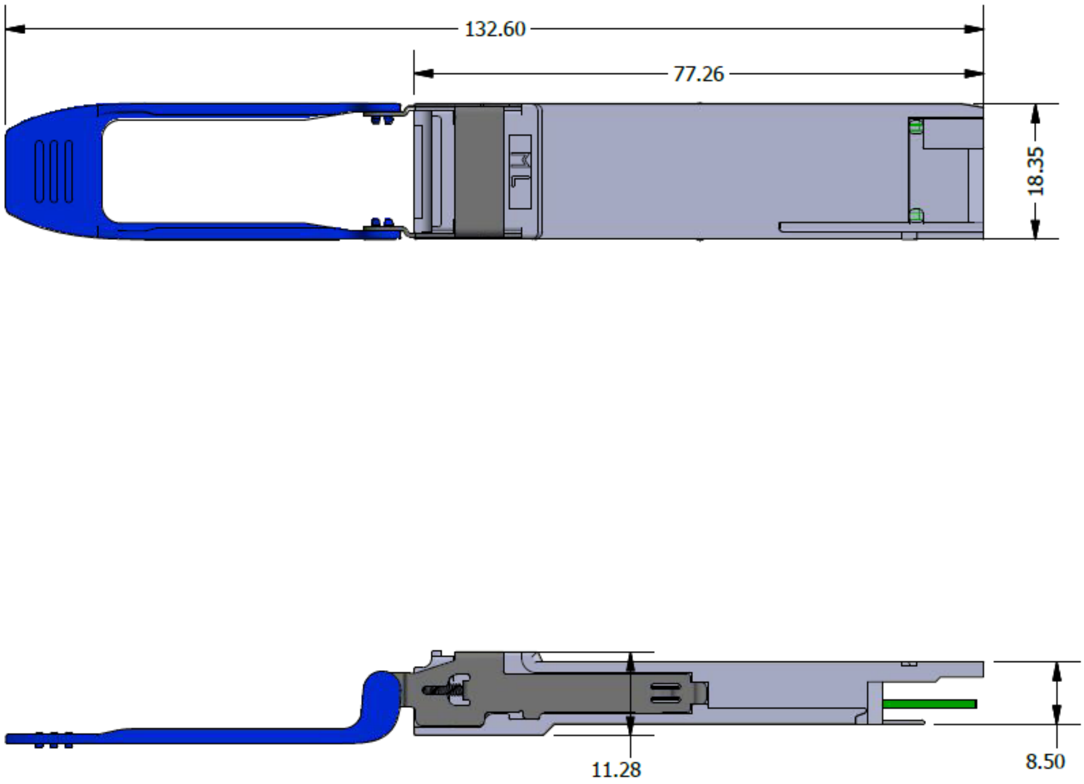

Figure 9: Mechanical Dimensions

Revision History

Revision number	Date	Description
0.1	6/22/2020	▪ Preliminary
0.2	11/9/2020	▪ Update format ▪ Update features list
0.3	6/23/2021	▪ Update “Operating Conditions” table
0.31	9/20/2021	▪ Format updates

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